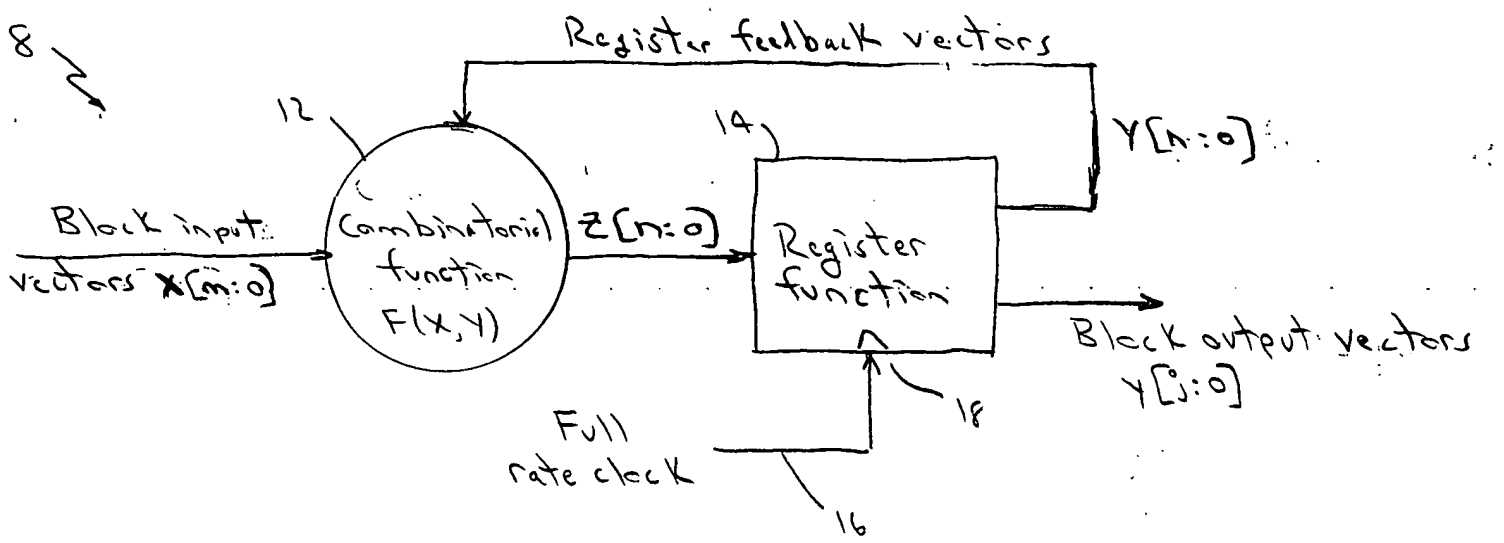

Figure 1 (Prior Art)

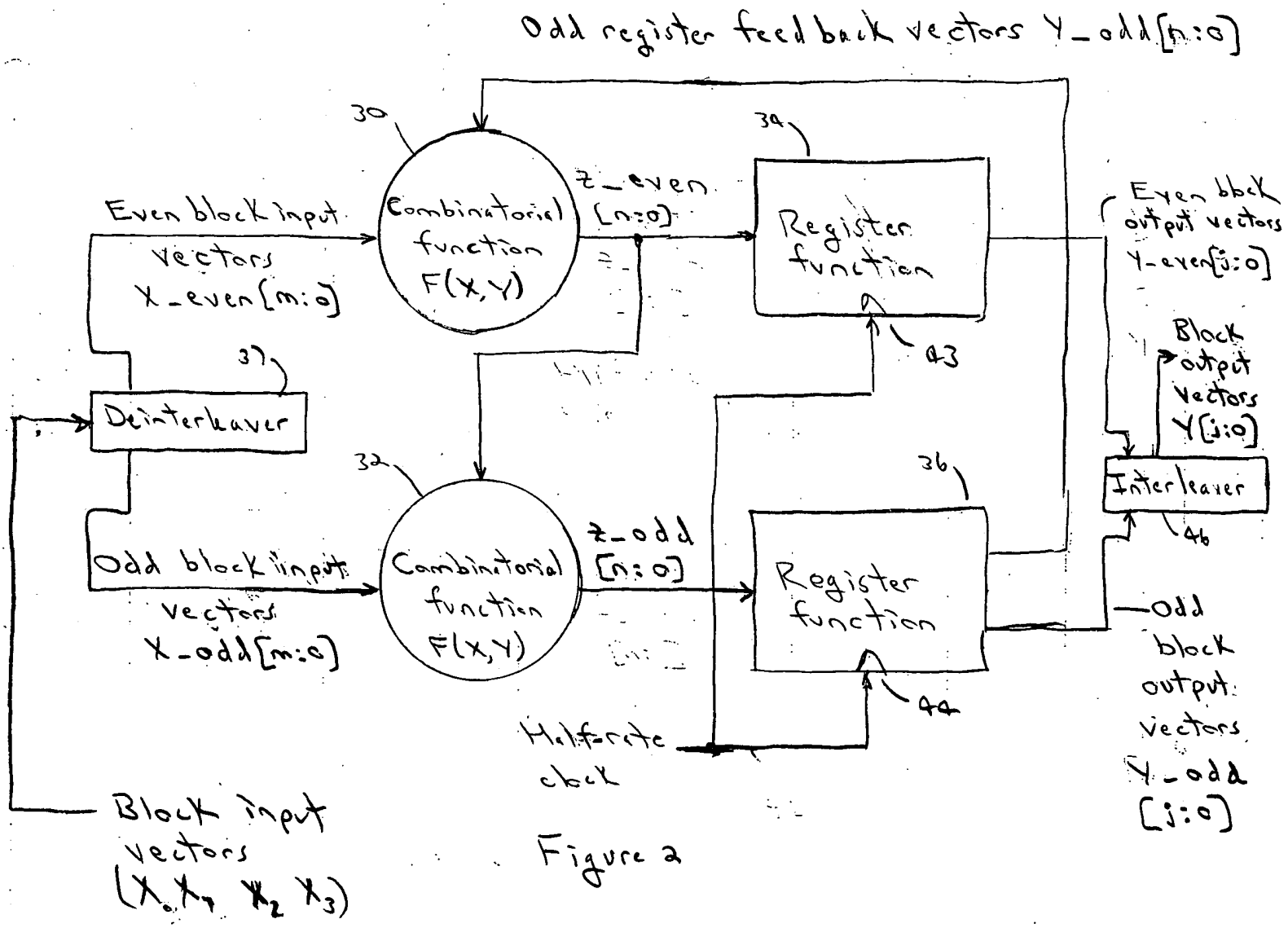

Figure 2

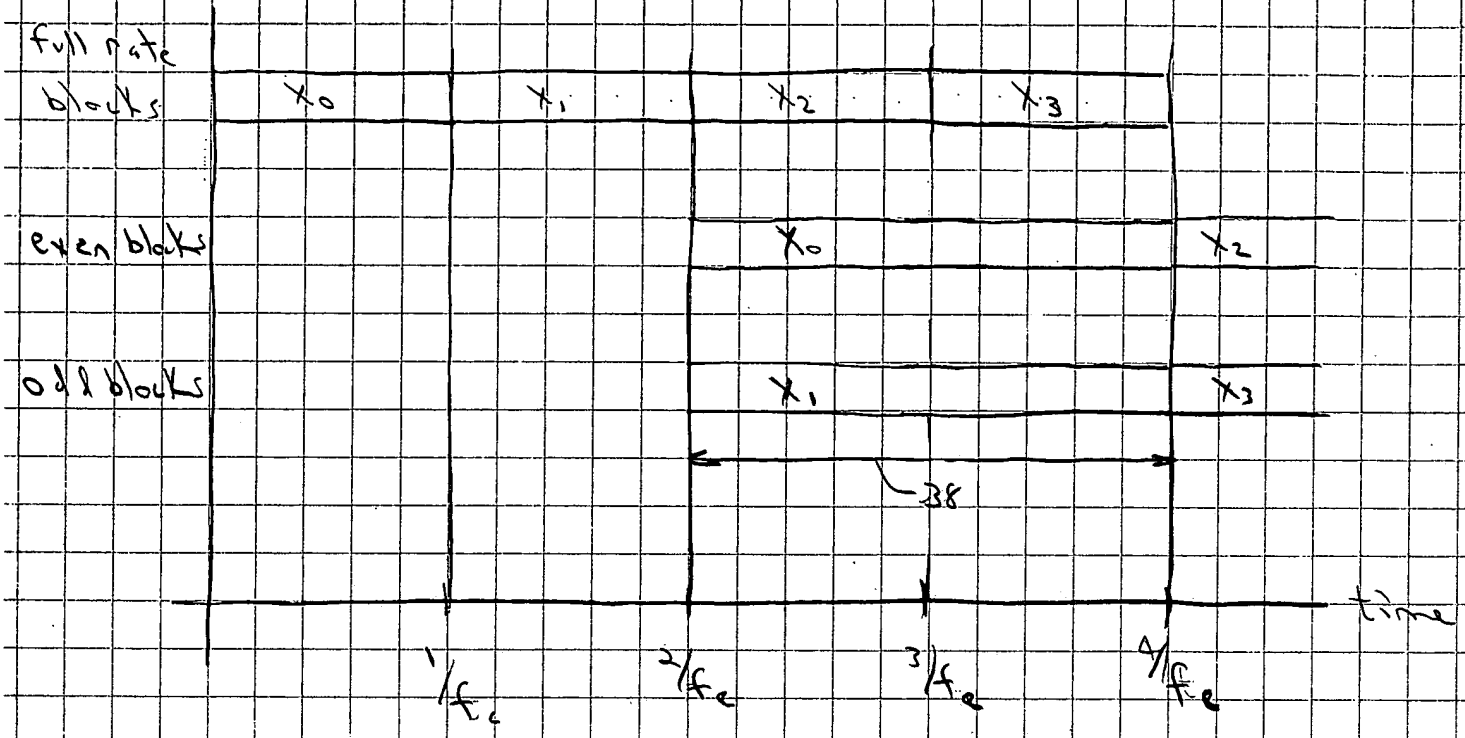
full rate blocks
X_0
X_1
X_2
X_3
even blocks
X_0
X_2
odd blocks
X_1
X_3
38
time
$1/f_c$
$2/f_c$
$3/f_c$
$4/f_c$

Figure 3

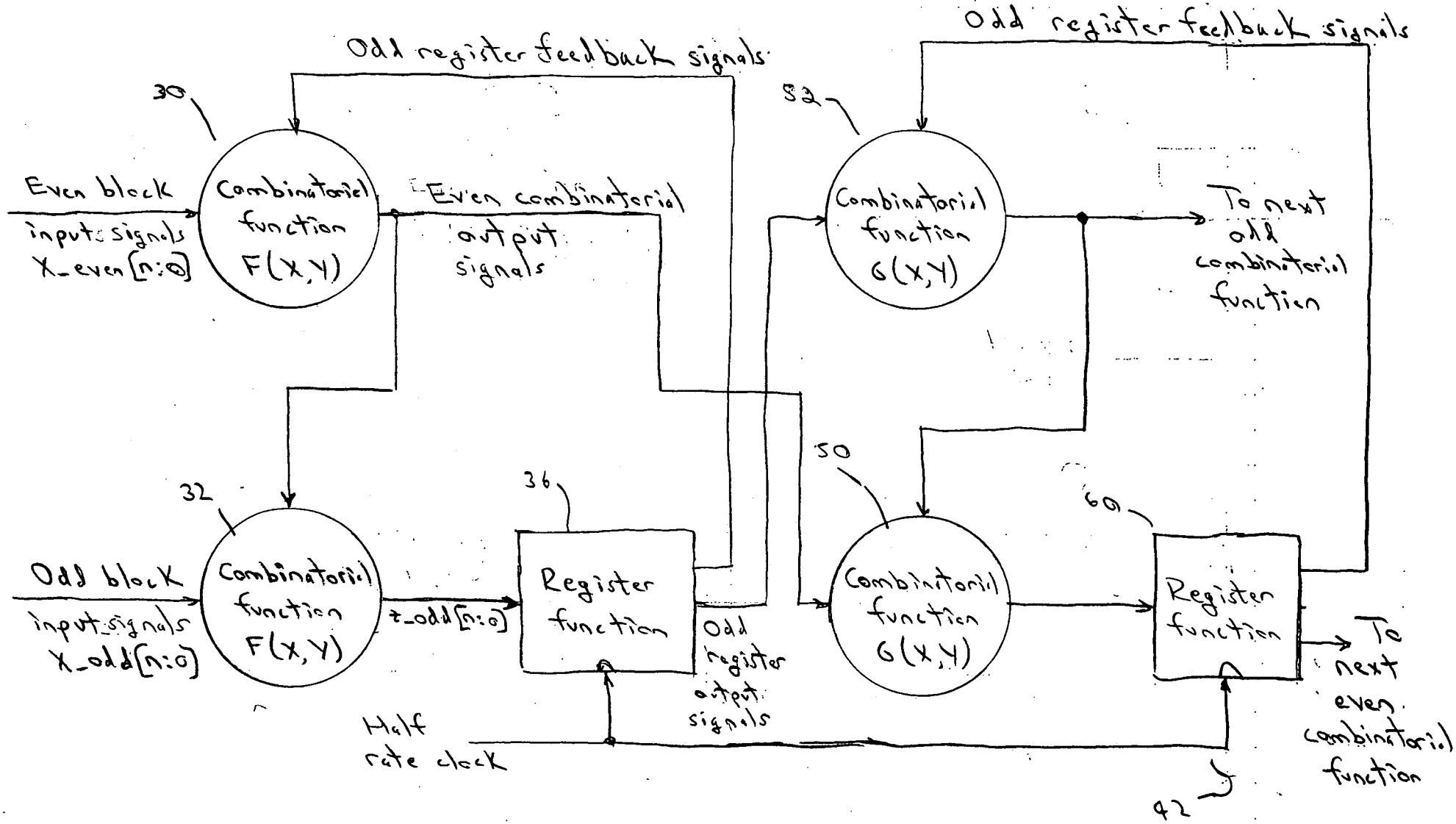
Odd register feedback signals
Odd register feedback signals
30
32
36
50
52
60
Even block
input signals
X_even[n:0]
Combinatorial
function
F(X,Y)
Even combinatorial
output
signals
Combinatorial
function
G(X,Y)
To next
odd
combinatorial
function
Odd block
input signals
X_odd[n:0]
Combinatorial
function
F(X,Y)
z_odd[n:0]
Register
function
Odd
register
output
signals
Combinatorial
function
G(X,Y)
Register
function
To
next
even
combinatorial
function
Half
rate clock
42

Figure 4

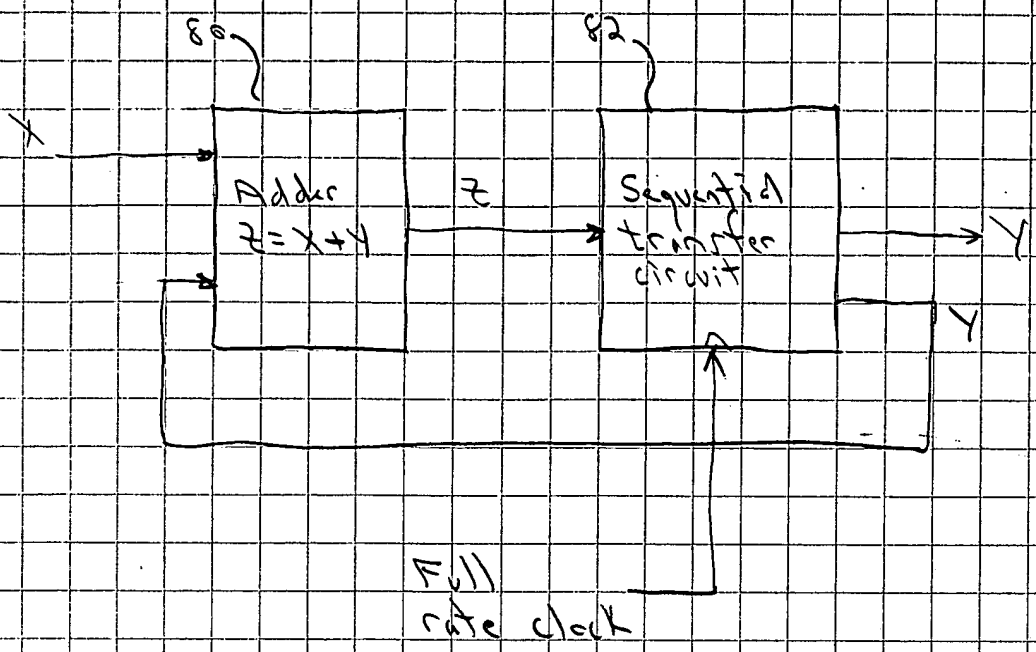

Figure 5

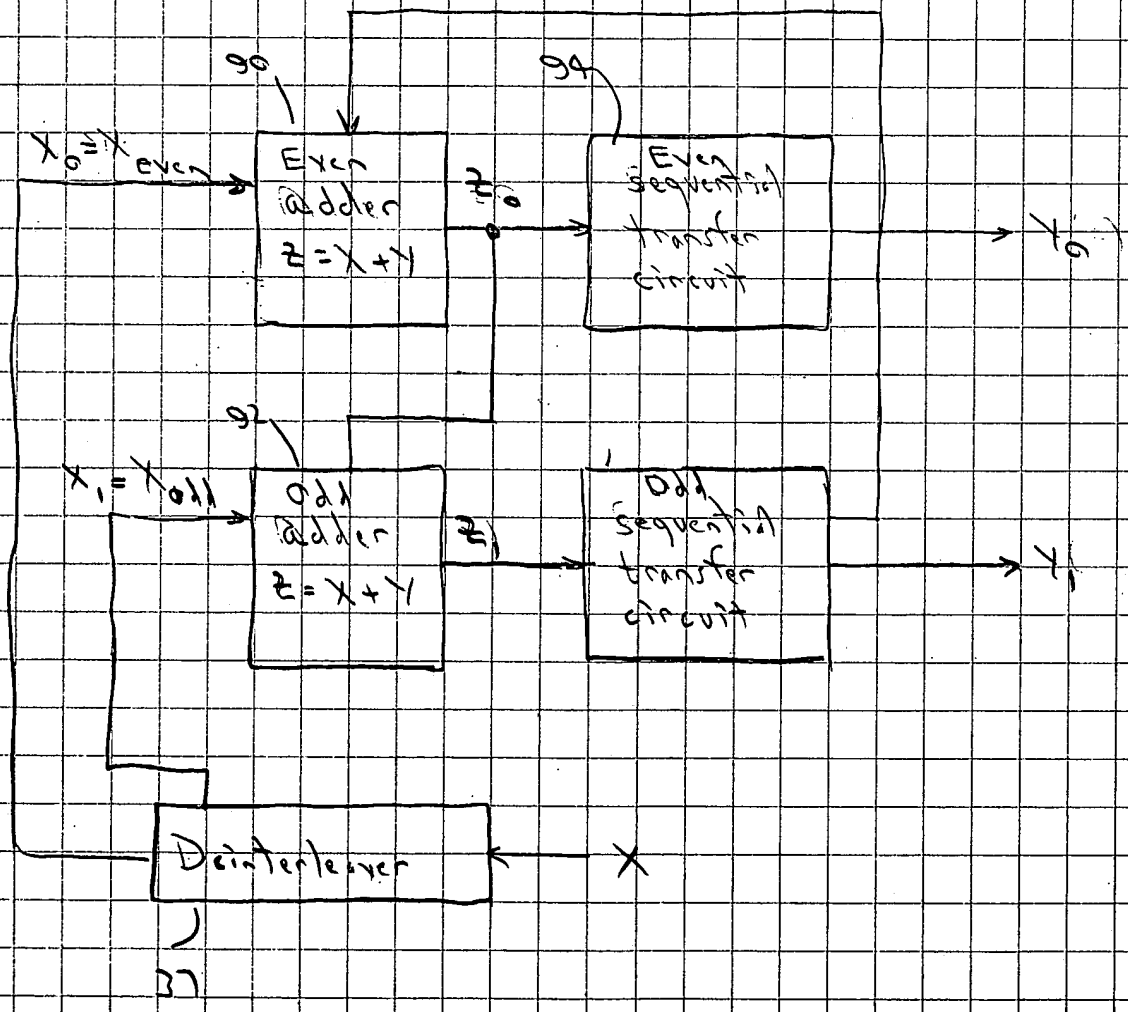

Figure 6

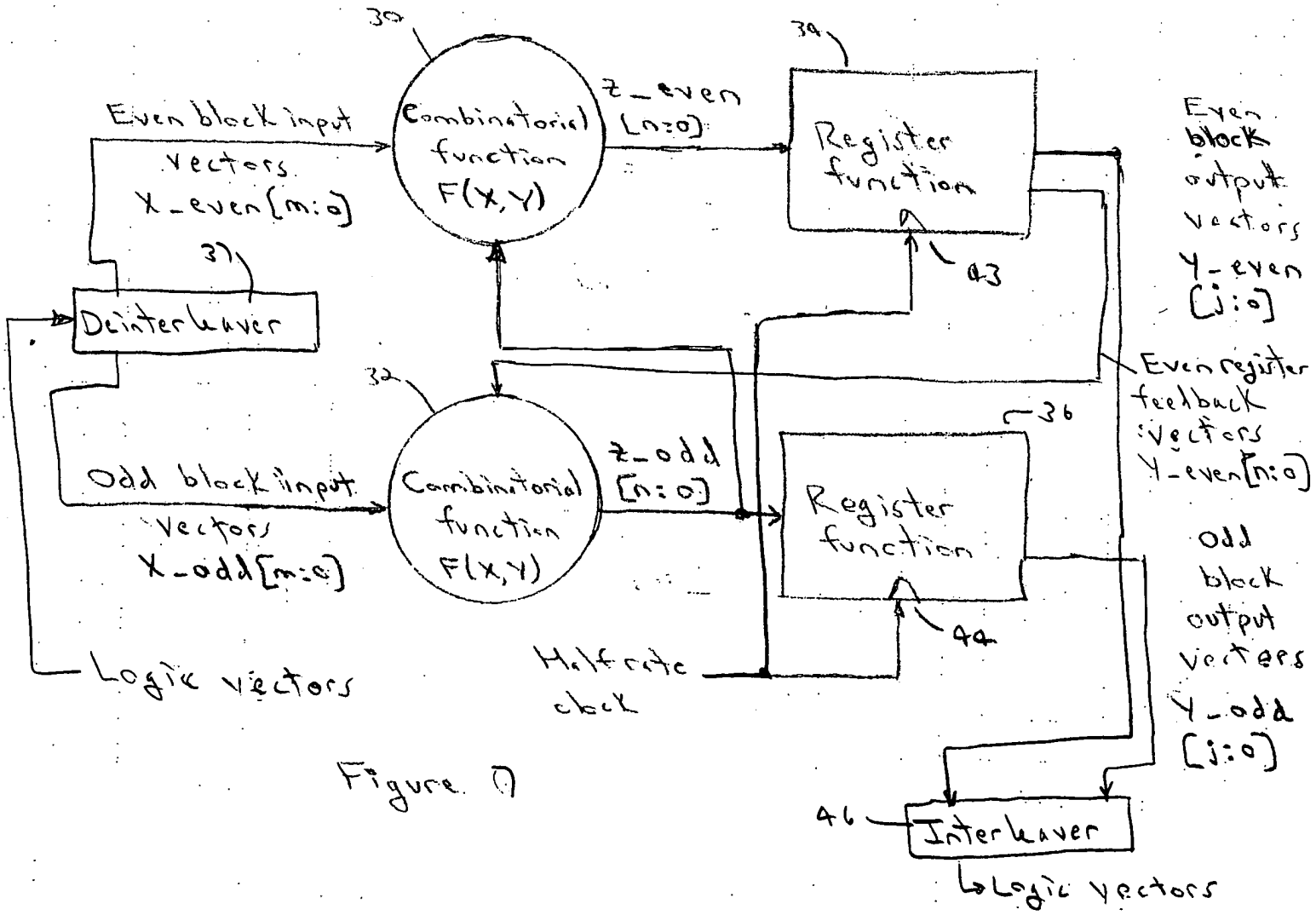
30
Even block input vectors X_even[m:0]
Combinatorial function F(X,Y)
Z_even [n:0]
39
Register function
43
Even block output vectors Y_even [j:0]
37
Deinterleaver
Even register feedback vectors Y_even[n:0]
32
Odd block input vectors X_odd[m:0]
Combinatorial function F(X,Y)
Z_odd [n:0]
36
Register function
44
Logic vectors
Half rate clock
Odd block output vectors Y_odd [j:0]
46
Interleaver
Logic vectors

Figure 1

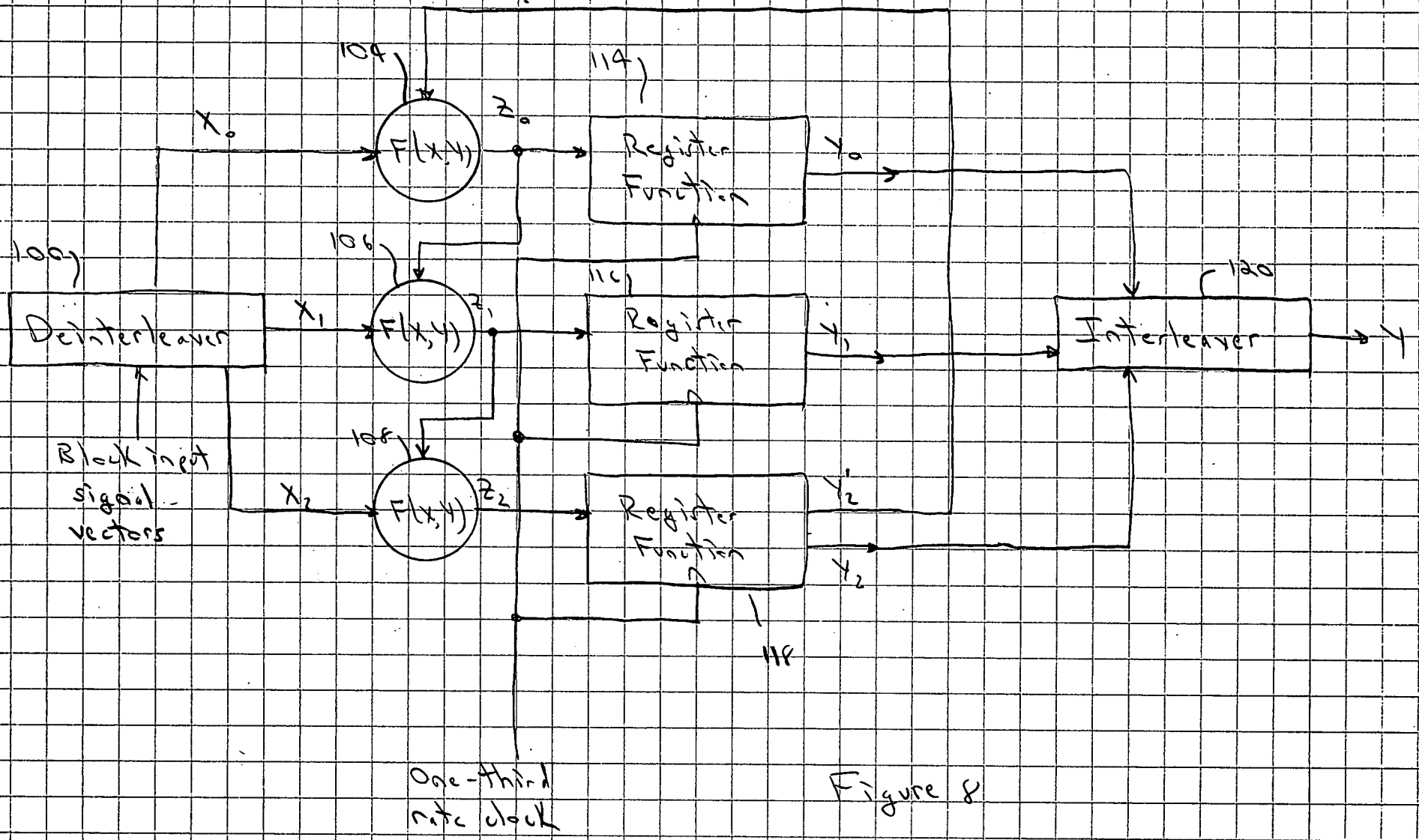
104
114
X_0
Z_0
F(X,Y)
Register Function
Y_0
100
106
110
120
Deinterleaver
X_1
Z_1
F(X,Y)
Register Function
Y_1
Interleaver
Y
108
Block input signal vectors
X_2
Z_2
F(X,Y)
Register Function
Y_2'
Y_2
118
One-third rate clock signal

Figure 8